AD9361 Reference Clock Requirements

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REVISION HISTORY

Version 2.0, October 6, 2011

GENERAL DESCRIPTION

The AD9361 Reference Clock Requirements document details connecting an external clock source to the AD9361 to meet parametric requirements.

CONNECTIONS FOR EXTERNAL CLOCK (MASTER CLOCK)

A Master Clock needs to be connected to XTALN (ball M12). Master Clock should be AC coupled to XTALN and XTALP (ball M11) is not connected (leave floating) for part revisions R1 and higher. The Master Clock frequency must be between 5MHz and 320MHz and can be scaled by 1x, ½ x, ¼ x and 2x using BBPLL, Rx and Tx reference dividers (registers 0x045, 0x2AB and 0x2AC respectively). The valid frequency range for the PLL phase detectors is 10MHz to 80MHz and the scaled frequency of the Master Clock must be within this range. The recommended range for the RF PLLs for optimum phase noise is 40MHz – 80MHz.

The level for the signal should be 1.3V pk-pk maximum (lower swings can be used but will limit performance). This signal can be a clipped sinewave or a CMOS signal. The best performance will be seen with the highest slew rate possible.

The XTALN (ball M12) has an input resistance of ~ 10kohms in parallel with 10pF. When using the XTALN pin (ball M12) the XTALP pin (ball M11) is not connected (leave floating).

EXTERNAL CLOCK PHASE NOISE

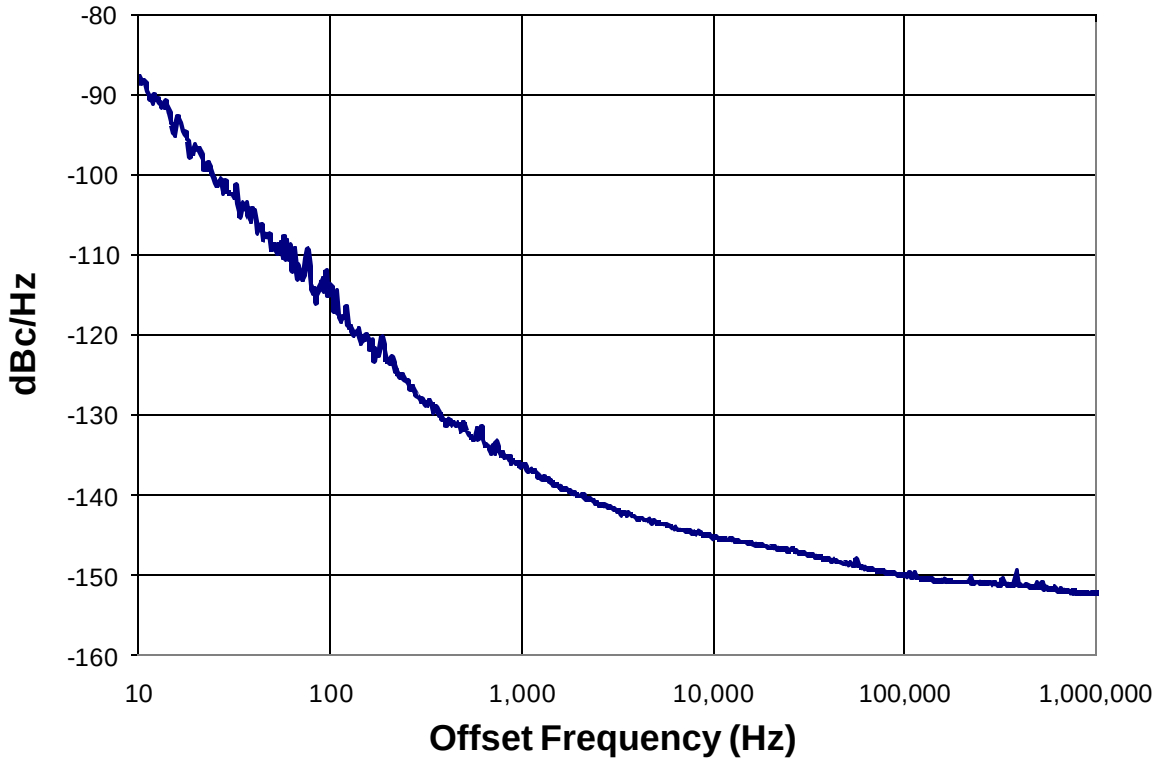

Figure 1 Expected SSB Phase Noise of External Clock measured at 40MHz fundamental frequency